Remarks

As discussed below, the rejections of claims 1-15 are improper because neither the '283 reference nor the '511 reference teach or suggest the claimed invention. Moreover, Applicant respectfully traverses the finality of the instant Office Action and submits that Applicant should be afforded an opportunity to respond by way of a new non-final Office Action. Specifically, the Examiner has improperly presented § 102(b) rejections based on the '283 reference and the '511 reference for the first time (*i.e.*, new grounds of rejection) in the form of a final rejection. *See, e.g.,* M.P.E.P. § 706.07(a). As should be apparent by the following discussion, a clear issue has not been established between Applicant and the Examiner and thereby an Appeal would be premature. "The examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal." M.P.E.P. § 706.07.

The Office Action dated January 15, 2009 lists the following new grounds of rejection: claims 1-4, 6, 8 and 12 stand rejected under 35 U.S.C. § 102(b) over Krakauer (U.S. Patent No. 5,617,283); claims 1-3 and 11 stand rejected under 35 U.S.C. § 102(b) over John (U.S. Patent No. 6,522,511); claims 5 and 7stand rejected under 35 U.S.C. § 103(a) over the '283 reference; claim 10 stands rejected under 35 U.S.C. § 103(a) over the '283 reference in view of Ker (U.S. Patent Pub. 2002/0050615); claims 11 and 15 stand rejected under 35 U.S.C. § 103(a) over the '283 reference in view of Lai (US Patent Pub. 2003/0235022); and claims 12-15 stand rejected under 35 U.S.C. § 103(a) over the '511 reference in view of Avery (U.S. Patent No. 6,501,632). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant first addresses a general failing of the rejections and then specifically addresses each rejection. Applicant respectfully submits that the newly presented rejections rely upon an interpretation that is inconsistent with the teachings of the references and Applicant's specification and that is contrary to how the skilled artisan would interpret the limitations. The unreasonableness of the Examiner's interpretation is highlighted by the attempt to assert that a wire connection (assumed by the teachings to have effectively zero resistance) and a transistor (specifically taught by the '283 reference

to be configured not to act as a capacitor) function as resistive and capacitive components of a time-delay circuit/means (*see, e.g.*, the interpretation of claim 4 on pages 2-3 of the instant Office Action). In pertinent part, the Examiner is of the opinion that transistor 42 is functioning to provide a capacitive function of a time-delay means and that a connection wire is functioning to provide a resistive function of the time-delay means. As explained by the '283 reference, transistor 42 is specifically configured to provide a high resistance/impedance (*see, e.g.*, Col. 4:21-29). Moreover, the skilled artisan, upon viewing the circuit design of transistor 42, would understand the purpose and function of the transistor 42 is not to provide any meaningful level of capacitance. Applicant further submits that the skilled artisan understands that the resistance in a circuit wire is assumed to be *de minimis* unless expressly discussed. To assert otherwise is contrary to Applicant's Specification, the teachings of the cited references and the general terminology and understanding of the skilled artisan.

The skilled artisan understands that there is some level of *de minimis* resistance, capacitance and inductance in all circuits. Nevertheless, the evidence of record does not mention these *de minimis* components of a circuit. Applicant submits that, unless expressly discussed, it is conventional for the skilled artisan to assume that a resistive, capacitive or inductive element is significantly more than these *de minimis* components. Both the cited references and Applicant's specification are consistent with this conventional use of terminology. Moreover, while the prosecution of other patents is not necessarily dispositive, Applicant requests that the Examiner consider the consequences of using such overly-broad and unreasonable interpretations. Using the Examiner's logic, the validity of a huge volume of issued patent claims that rely upon otherwise novel applications of resistive, capacitive and/or inductive elements would suddenly be called into question.

Applicant respectfully traverses the § 102(b) rejection of claims 1-4, 6, 8 and 12 because the cited portions of the '283 reference do not correspond to aspects of the claimed invention directed to a time-delay circuit/means that includes a resister and a capacitive device connected in series between a power supply and control inputs of first and second transistors. The Examiner erroneously asserts that the "connection means" between transistor 42 (*i.e.*, the asserted capacitive device) and signal line 16 (*i.e.*, the asserted power

supply) correspond to Applicant's resister. The Examiner's assertion of correspondence violates M.P.E.P. § 2111, which requires that the claims be given their broadest reasonable construction in light of Applicant's specification as it would be interpreted by one of ordinary skill in the art. Applicant submits that simply because "connection means" (*e.g.*, wires) have some (nominal) resistance does not mean that the skilled artisan would interpret a wire as corresponding to a resister. The skilled artisan, in view of Applicant's specification (*see, e.g.*, Figure 2 and paragraph 0034), would interpret the resister of the claimed invention as being an element that effects the operation of a circuit, in contrast to the "connection means," which have a nominal impact on the operation of the circuit. As such, the skilled artisan, in view of Applicant's specification, would not interpret the "connection means" of the '283 reference as being a resister. Accordingly, the Examiner's interpretation of the claimed invention violates M.P.E.P. § 2111.

Moreover, the cited portions of the '283 reference do not teach that transistor 42 (*i.e.*, the asserted capacitive device) is connected to a power supply, and, in fact, the '283 reference teaches away from connecting transistor 42 to a power supply. Instead the cited teachings of the '283 reference indicate that transistor 42 is connected to signal line 16. In fact, the '283 reference teaches that the embodiment disclosed in Figure 2 eliminates the need for a reference supply voltage (*e.g.*, V_{DD}) to be available for the modulation circuit 40. *See, e.g.*, Col. 4:59-67. As such, the '283 reference teaches away from connecting transistor 42 to a power supply. *See, e.g., KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) (In *KSR*, the Supreme Court looked favorably on *Adam's* treatment of teaching away stating, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.")

In view of the above, the cited portions of the '283 reference do not correspond to the claimed invention. Accordingly, the § 102(b) rejection of claims 1-4, 6, 8 and 12 is improper and Applicant requests that it be withdrawn. The § 103(a) rejections of claims 5, 7, 10-11 and 15 based on the '283 reference are also improper for at least the reasons discussed above and Applicant requests that they be withdrawn.

Applicant respectfully traverses the § 102(b) rejection of claims 1-3 and 11 because the cited portions of the '511 reference do not correspond to aspects of the claimed invention directed to a time-delay means that includes a resister and a capacitance connected

in series between a supply voltage terminal and control inputs of first and second transistors. The Examiner once again improperly asserts that "connection means" in a circuit correspond to a separate circuit element, specifically, that "the line capacitance of the connection means of R of 30 in Figure 3" correspond to Applicant's capacitance. The Examiner's interpretation of the claimed invention essentially gives no meaning to the claimed capacitance and, as discussed above, such an interpretation violates M.P.E.P. § 2111 (The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art."). Accordingly, the § 102(b) rejection of claims 1-3 and 11 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 12-15 because the cited combination does not correspond to aspects of the claimed invention directed to a time-delay circuit that includes a resister and a capacitive device connected in series between a power supply and control inputs of first and second transistors. The Examiner acknowledges that the '511 reference does not teach or suggest a time-delay circuit connected as in the claimed invention. The Examiner then erroneously asserts that the '632 reference teaches that resister R_{Z1} and capacitor C are connected in series between pad 301 and the control input of the NMOS transistor. *See, e.g.,* Figure 3. In actuality, the '632 reference teaches that resister R_{Z1} is the internal (or parasitic) resistance of Zener diode Z1, and that an alternative to using Zener diode Z1 is to use capacitor C (shown in phantom in Figure 3) in lieu of the diode Z1. *See, e.g.,* Col. 3:5-6 and Col. 3:56-61. Thus, the '632 reference teaches that either Zener diode Z1 (*i.e.,* resister R_{Z1}) or capacitor C is connected between pad 302 and the control input of the NMOS transistor, not both. The Examiner, in the instant Office Action, continues to assert that the '632 reference "teaches that Z1 can be replaced by a capacitance, to result in Rz1 and C in series." However, the Examiner's position is directly contradicted by the express teachings of the '632 reference, which state that the resister R_{Z1} is the internal resistance of diode Z1 and thus resister R_{Z1} is no longer present in the circuit of Figure 3 when the diode Z1 is replaced by capacitor C. As such, the § 103(a) rejection of claims 12-15 fails to establish *prima facie* obviousness, based upon the lack of teaching or suggestion of all limitations.

Moreover, the '511 reference expressly teaches away from the asserted combination with the '632 reference. In *KSR,* the Supreme Court looked favorably on *Adam's* treatment of teaching away stating, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). The '511 reference expressly teaches that a capacitive device should not be used (*see, e.g.*, Col. 2:14-17). In addition, this is one of the primary objects of the '511 reference and the proposed modification would render the circuit of the '511 reference unsuitable for use in high-speed digital circuitry. "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." M.P.E.P. § 2143.01. Accordingly, the § 103(a) rejection of claims 12-15 is improper and Applicant requests that it be withdrawn.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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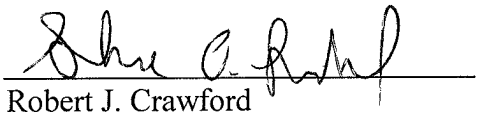
By: 

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